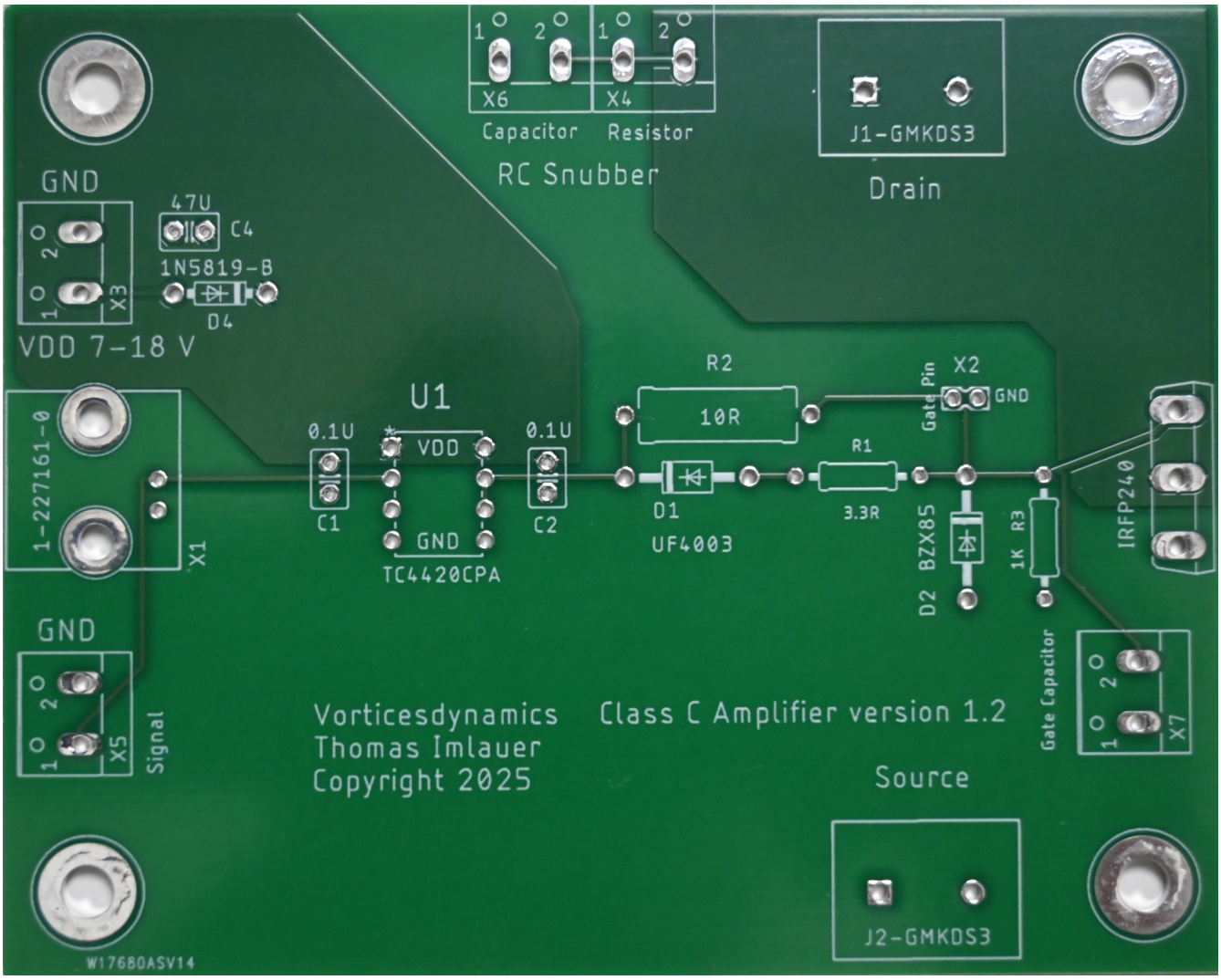
CLASS C AMPLIFIER - VERSION 1.2

TC4420 MOSFET driver and switching board | Vorticesdynamics | Thomas Imlauer | Copyright 2025



FUNCTION The board converts an external pulse or square-wave signal into a high-current gate-drive signal using the TC4420CPA. The driver switches an IRFP240 power MOSFET in Class C or pulsed operation. The drain and source terminals connect the MOSFET to the external load circuit, while the gate network, optional gate capacitor and RC snubber control switching speed, ringing and voltage overshoot.

CONNECTIONS

Ref.	Connection	How to wire
X3	VDD input	Pin 1: +7-18 V DC; pin 2: GND.
X5	Signal input	Pin 1: pulse/square-wave signal; pin 2: signal GND.
J1	Drain	Connect to the switched side of the coil, transformer or resonant load.
J2	Source	Connect to the power-return/ground side of the external switching circuit.
X2	Gate test	Gate-pin and GND test points for oscilloscope measurement.
X7	Gate capacitor	Optional capacitor between gate and source/GND; fit only when required by the application.
X6/X4	RC snubber	Fit the snubber capacitor at X6 and resistor at X4. Values are load-dependent.
X1	Aux. footprint	Optional 2-pin connector footprint. Use only according to the board schematic/application wiring.

BASIC WIRING SEQUENCE

- Populate and inspect all components before applying power.
- Connect X3 to a regulated 7-18 V DC driver supply.
- Connect the signal generator to X5 with a common ground.
- Connect J2 to circuit return and J1 to the load switching node.
- Start with low voltage, low duty cycle and no resonant overvoltage. Verify the gate waveform at X2 before full-power operation.

COMPONENT FUNCTIONS

U1 - TC4420CPA: High-current, non-inverting MOSFET gate driver.
Q1 - IRFP240: N-channel power MOSFET; requires a suitable heatsink.
C1, C2 - 0.1 µF: Local high-frequency supply decoupling at U1.
C4 - 47 µF: Driver-supply bulk decoupling.
D4 - 1N5819: Supply protection/isolation diode in the VDD input section.
R1 - 3.3 Ω: Series gate resistor limiting peak gate current and ringing.
R2 - 10 Ω / D1 UF4003: Asymmetric gate charge/discharge shaping network.
D2 - BZX85: Gate-voltage clamp; select the specified Zener voltage for the design.
R3 - 1 kΩ: Gate-to-source pull-down, keeping Q1 off without drive.
X7: Optional gate-to-source capacitor position.
X4 + X6: Series RC snubber positions for the drain switching node.

OPERATING NOTES

- The board supply powers the TC4420 gate-driver section; load power and allowable drain voltage/current are determined by the external circuit and MOSFET ratings.
- Keep the signal and gate loops short. Keep drain/load wiring separated from the low-level signal wiring.
- The IRFP240 tab is electrically connected to the drain. Use an insulating pad if the heatsink must not be at drain potential.
- Choose RC snubber and gate-capacitor values from measured waveforms; incorrect values can increase dissipation.
- Resonant loads can generate voltages far above the DC supply. Disconnect power and discharge capacitors before touching the circuit.

CAUTION: This is an experimental switching board, not a complete protected power supply. Confirm component orientation, grounding, heatsinking and voltage ratings before operation.